

REMARKS

Now in the application are Claims 1-50 of which Claims 1, 21, 22, 28, 29, and 49 are independent. Claims 1-20 and 29-48 have been allowed. Claims 21-28, 49, and 50 have been rejected. The following comments address all stated grounds for rejection and place the presently pending claims, as identified above, in condition for allowance.

ALLOWABLE SUBJECT MATTER

The Examiner has allowed claims 1-20 and 29-48. Applicants would like to thank the Examiner for allowing these claims.

SPECIFICATION

The title of the invention stands objected to as non-descriptive. In the response accompanying the Request for Continued Examination (RCE) filed on April 12, 2005 Applicants amended the title to add further descriptive language as requested by the Examiner. Applicants respectfully submit that the amended title does describe the invention. Accordingly, Applicants respectfully request the Examiner to reconsider and withdraw the objection to the specification.

CLAIM OBJECTIONS

Claims 5-17, 19-20, 34-45, 47, and 48 stand objected to for improper dependent form. MPEP §608.01(n) is cited in support of the objection. Nevertheless, Applicants respectfully choose to defer the renumbering of the Claims until all allowable subject matter is identified to avoid further confusion during prosecution. Accordingly, Applicants respectfully request the Examiner to continue the objection under MPEP §608.01(n).

CLAIM REJECTIONS UNDER 35 U.S.C. §103

Claims 21-28, 49-50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yeager (patent No. 5,758,112) in view of Rodgers (patent No. 6,889,319). Applicants respectfully traverse this rejection on the basis of the following arguments.

Summary of Yeager (patent No. 5,758,112)

The Yeager patent is directed to a method and apparatus for storing register renaming information in the event of a branch misprediction. Yeager discloses redundant mapping tables for use in microprocessors that rename registers and perform branch prediction. The redundant mapping tables include a number of primary RAM cells coupled to a number of redundant RAM cells. In the event of a branch instruction, the redundant RAM cells can save the contents of the primary RAM cells in a single clock cycle before the microprocessor decodes and executes subsequent instructions along a predicted branch path. Should the branch instruction be mispredicted, the redundant RAM cells can restore the primary RAM cells in a single clock cycle. To accomplish this, Yeager discloses a free register list coupled to a mapping table, which in turn is coupled to an instruction queue and the instruction queue is coupled to a register file. The free register lists disclosed by Yeager each include a read pointer and write pointer to identify entries in selected RAMs. Yeager moves the write pointer in increments determined by the member of instructions which graduate during each clock cycle. Likewise, Yeager moves the read pointer in increments by the number of free registers assigned during each clock cycle. .

Summary of Rodgers (patent No. 6,889,319)

The Rodgers patent is directed to method for maintaining a state machine to provide a multi-bit output, each bit of the multi-bit output indicating a respective status for an associated thread of multiple threads being executed within a multithreaded processor. Status for a first thread is detected, responsive to which a functional unit within the multithreaded processor is configured in accordance with the multi-bit output of the state machine.

A. Rejection of Claim 21 Under 35 U.S.C. §103:

The Office Action rejects Claim 21 as being unpatentable over Yeager in view of Rodgers. Applicants respectfully traverse this rejection on the basis of the following arguments, and further contend that neither Yeager nor Rodgers teach or suggest all of the elements of this claim as described below.

The Yeager patent discloses two independent free register lists for managing register allocation. Nowhere does Yeager disclose the tracking of two sets of pointers in a single structure. The Examiner has admitted to as much.

Rodgers does not cure this deficiency of Yeager. Figure 8 and 9 of Rodgers indicated by the Examiner illustrate a reorder buffer. This reorder buffer is not the same as a register. Indeed the register list is a separate entity in Rodgers (block 124 in Fig. 4). The reorder buffer does not track register allocation as set forth in Claim 21. The reorder buffer also does not have a set of pointers to manage the register allocation for an instruction as set forth in Claim 21. As such, Rodgers, alone or in combination with Yeager, fails to teach or suggest all the limitations of Claim 21.

Also there is not motivation to combine Yeager and Rodgers. Those skilled in the art along with the prior art teach placement of separate and distinct dedicated structures for managing registers in close proximity to respective array structures to facilitate association of physical registers with logical registers and hence facilitate operational performance of a superscalar processor. As discussed in the previous response, as processors have become larger and more complicated, internal data and program storage in the form of register files and cache arrays consume an increasing portion of the transistor count and die area. Consequently performance, power, yield, and reliability of the overall die is greatly influenced by the design of the structures holding physical registers and the design of structures used to track register allocation for multiple threads of the processor. Speculative processors utilize a load store architecture that typically requires a large number of general purpose registers. Performance boost innovations such as register renaming and register windowing further expand the number of general purpose registers.

Typically, the general purpose register arrays are located inside the data paths of execution units. Consequently, the register file layout must occur on the same pitch as the data path. Because the data path pitch is wider than a typical SRAM cell, the register can use devices that are larger than typically used in large SRAM design. Thus, some of the issues typically associated with SRAM design are reduced. The Yeager patent teaches such an architecture by placing register files 302 and 306 inside the data path of respective execution units. Consequently, the architecture, function, and operation of a superscalar processor as disclosed by Yeager having two separate and distinct caches of general purpose registers to facilitate operational performance teaches that each register array requires in close proximity thereto a dedicated structure for managing free registers. Hence, Yeager discloses a floating point free register list 208 separate and distinct from the integer free register list 210. Yeager has separate registers for the independent floating point and integer processing path. The floating point and integer processing do not share a register and as such don't require increased utilization of a shared resource as taught by Rogers.

Accordingly, Applicants respectfully request the Examiner to reconsider and withdraw the rejection of Claim 21 under 35 U.S.C. §103.

B. Rejection of Claims 22-27 Under 35 U.S.C. §103:

The Office Action rejects Claims 22-27 as being unpatentable over Yeager in view of Rodgers. Applicants respectfully traverse this rejection on the basis of the following arguments.

Yeager fails to teach or suggest a retire pointer as set forth in claim 22. Yeager discloses a read pointer and a write pointer, however, Yeager does not disclose a retire pointer. The Yeager patent discloses a graduation mask used to identify which instruction graduated. A mask is not a pointer. The Examiner has admitted to as much. The addition of Rodgers fails to cure this deficiency.

As with above, the section of Rodgers the Examiner has cited deals with a reorder buffer. As discussed above, the reorder buffer is a separate and independent element from the register list. As such, the retirement pointer does not identify where a pointer pointing to at least one of said

plurality of physical registers assigned as a destination register for an instruction in said first thread that is next to be retired. Therefore, Rodgers, alone or in combination with Yeager, fails to teach or suggest all the limitations of claim 22.

Claims 23-27 depend, directly or indirectly upon Claim 22 and therefore incorporate the limitations of Claim 22.

Accordingly, Applicants respectfully request the Examiner to reconsider and withdraw the rejection of Claims 22-27 under 35 U.S.C. §103.

C. Rejection of Claim 28 Under 35 U.S.C. §103:

The Office Action rejects Claim 28 as being unpatentable over Yeager in view of Rodgers. Applicants respectfully traverse this rejection on the basis of the following arguments.

Claim 28 is directed to a semiconductor device having a number of physical registers that are assigned as destination registers for instructions to be executed by a microprocessor performing out of order execution. The semiconductor device includes a first module providing a structure for holding information identifying available physical registers of the microprocessor, a first set of register pointers assigned to a first portion of the structure and a second set of registers assigned to a second portion of the structure. As stated in the previous response, the Yeager patent does not anticipate Claim 28.

The Yeager patent discloses a first structure for holding information identifying available physical registers in a floating point instruction pipeline and a second structure for identifying available physical registers and a second pipeline or integer instruction pipeline of the microprocessor. In contrast, the semiconductor device of Claim 28 discloses a structure partitionable to hold at least two sets of register pointers to track the assignment of destination registers for at least two threads of a microprocessor performing out of order execution. Nowhere does the Yeager patent disclose a partitionable structure to track physical register assignments corresponding to either two threads or two instruction pipelines of a microprocessor. The Yeager

patent discloses a single structure for each thread or instruction pipeline that includes a set of register pointers assigned to track physical registers assigned as destination registers for instructions in each respective thread or instruction pipeline. Accordingly, the semiconductor device of the Yeager patent has an architecture and a structure along with a function and an operation different from the architecture, structure, function, and operation of the semiconductor device of Claim 28. Hence, the Yeager patent fails to teach or disclose each and every limitation of Claim 28.

As discussed above with regard to Claim 21, Rodgers does not cure this deficiency of Yeager. Figure 8 and 9 of Rodgers indicated by the Examiner illustrate a reorder buffer. This reorder buffer is not the same as a register. Indeed the register list is a separate entity in Rodgers (block 124 in Fig. 4). The reorder buffer does not hold information identifying available physical registers as set forth in Claim 28. The reorder buffer also does not have a set of pointers to track the physical registers assigned as the destination registers for a thread as set forth in Claim 21. As such, Rodgers, alone or in combination with Yeager, fails to teach or suggest all the limitations of claim 21.

Accordingly, Applicants respectfully request the Examiner to reconsider and withdraw the rejection of Claim 28 under 35 U.S.C. §103.

D. Rejection of Claim 49 Under 35 U.S.C. §103:

The Office Action rejects Claim 49 as being unpatentable over Yeager in view of Rodgers. Applicants respectfully traverse this rejection on the basis of the following arguments.

Claim 49 is directed to a computer readable medium holding computer executable instructions for performing a method in a multithreading processor performing speculative instruction execution. Performance of the method provides a single structure to track register allocation for a first thread and a second thread of the multithreading microprocessor. The method includes a step of tracking a first set of pointers in the structure assigned to manage register allocation of an instruction of the first thread of the multithreading processor and includes a step of tracking a second set of pointers in the structure assigned to manage the register allocation of an

instruction of the second thread of the multithreading processor. Claim 49 is not taught or suggested by Yeager.

The Yeager patent discloses two independent free register lists for managing register allocation. Specifically, free register list (208) manages registers associated with floating point instructions and free register list (210) manages registers associated with integer related instructions. Nowhere does Yeager disclose that the floating point free register list and the integer free register list are a single structure. In contrast, amended Claim 49 recites a step of providing a single structure to track register allocation for a first thread and a second thread of the multithreading processor. Performance of the method recited in amended Claim 49 tracks at least two sets of pointers in the provided structure. As discussed in connection with the rejection of Claim 21, nowhere does Yeager disclose the tracking of two sets of pointers in a single structure. Yeager tracks one set of pointers in a first structure and a second set of pointers in a second structure. Accordingly, the microprocessor disclosed by the Yeager patent has an architecture, operation, and function different from the architecture, function, and operation of the method performed in a multithreading microprocessor performing speculative instruction execution recited in Claim 49.

As with claim 21, Rodgers does not cure this deficiency of Yeager. Figure 8 and 9 of Rodgers indicated by the Examiner illustrate a reorder buffer. This reorder buffer is not the same as a register. Indeed the register list is a separate entity in Rodgers (block 124 in Fig. 4). The reorder buffer does not track register allocation as set forth in Claim 21. The reorder buffer also does not have a set of pointers to manage the register allocation for an instruction as set forth in Claim 21. As such, Rodgers, alone or in combination with Yeager, fails to teach or suggest all the limitations of Claim 21.

Accordingly, Applicants respectfully request the Examiner to reconsider and withdraw the rejection of amended Claim 49 under 35 U.S.C. §103.

E. Rejection of Claim 50 Under 35 U.S.C. §103:

The Office Action rejects Claim 50 as being unpatentable over Yeager in view of Rodgers. Applicants respectfully traverse this rejection on the basis of the following arguments.

Claim 50 depends from Claim 21 and as such incorporates each and every element of claim 21. As discussed above, the combination of Yeager and Rodgers fails to disclose each and every element of Claim 21. Thus Yeager and Rodgers fail to teach and disclose each and every element of Claim 50.

Accordingly, Applicants respectfully request the Examiner to reconsider and withdraw the rejection of amended Claim 50 under 35 U.S.C. §103.

CONCLUSION

In view of the remarks set forth above, Applicants believe that the present invention is in condition for allowance. If the Examiner deems there are any remaining issues, we invite the Examiner to call the undersigned at (617) 227-7400.

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Respectfully submitted,

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